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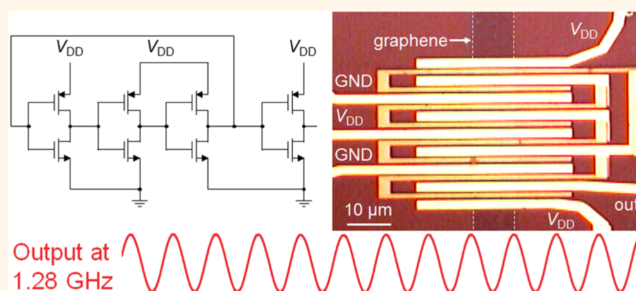
Gigahertz Integrated Graphene Ring Oscillators

Erica Guerriero,[†] Laura Polloni,[†,‡] Massimiliano Bianchi,[†] Ashkan Behnam,[§,⊥] Enrique Carrion,[§,⊥] Laura Giorgia Rizzi,[†] Eric Pop,[§,⊥,||] and Roman Sordan[†,*]

[†]L-NESS, Department of Physics, Politecnico di Milano, Polo di Como, Via Anzani 42, 22100 Como, Italy, [‡]Department of Science and High Technology, Universitá degli Studi dell'Insubria, Via Valleggio 11, 22100 Como, Italy, [§]Department of Electrical and Computer Engineering, University of Illinois at Urbana—Champaign, Urbana, Illinois 61801, United States, [⊥]Micro and Nanotechnology Lab, University of Illinois at Urbana—Champaign, Urbana, Illinois 61801, United States, and [||]Beckman Institute, University of Illinois at Urbana—Champaign, Urbana, Illinois 61801, United States

ABSTRACT Ring oscillators (ROs) are the most important class of circuits used to evaluate the performance limits of any digital technology. However, ROs based on low-dimensional nanomaterials (*e.g.*, 1-D nanotubes, nanowires, 2-D MoS_2) have so far exhibited limited performance due to low current drive or large parasitics. Here we demonstrate integrated ROs fabricated from wafer-scale graphene grown by chemical vapor deposition. The highest oscillation frequency was 1.28 GHz, while the largest output voltage swing was 0.57 V. Both values remain limited by parasitic capacitances in the circuit rather than intrinsic properties of the graphene transistor components, suggesting further improvements are possible. The fabricated ROs are the fastest realized in any low-dimensional nanomaterial to date and also the least sensitive to fluctuations in the supply voltage. They represent the first integrated graphene oscillators of any kind and can also be used in a wide range of applications in analog electronics. As a demonstration, we also realized the first stand-alone graphene mixers that do not require external oscillators for frequency conversion. The first gigahertz multitransistor graphene integrated circuits demonstrated here pave the way for application of graphene in high-speed digital and analog circuits in which high operating speed could be traded off against power consumption.



KEYWORDS: graphene · oscillator · logic gates · integrated circuit · voltage gain · digital electronics · analog electronics

Rapid progress of wireless, fiber-optic, and space communications has led to a growing need for digital systems capable of operating at extremely high frequency (EHF; f > 100 GHz) and signal processing at extremely high data transfer rates (>100 Gbit/s).[1] To this end, a special class of ultra-high-speed digital circuits has been developed in order to perform data conversion at the transmitting/receiving side of serial EHF lines, such that information carried by EHF digital signals can be processed at lower clock rates by low-power, highly integrated, and parallel Si complementary metal oxide semiconductor (CMOS) logic.[2] Graphene[3] could emerge as a possible contender in the ultra-high-speed circuit arena due to its very large charge carrier mobility.[4−6] Unlike other materials, the graphene mobility is equal between electrons and holes and much greater than that of InP, which currently dominates high-speed electronics.[1] The absence of a band gap in graphene, which represents a disadvantage in low-power digital applications, does not necessarily hinder high-speed circuits that achieve fast operation at the expense of a large static power dissipation and with reduced circuit complexity.[7] The power dissipation of graphene logic gates is similar to those of the fastest InP emitter coupled logic (ECL) gates,[2,8] even though graphene logic gates have larger voltage swing (as a fraction of supply voltage) than ECL gates.[9] However, only through further technological advances, some of which will be discussed here, may graphene be able to compete with or replace InP in EHF circuits.

Despite the high intrinsic cutoff frequency (f_T > 100 GHz) of individual graphene field-effect transistors (FETs),[10] no demonstrations exist yet of high-speed graphene digital circuits. This apparent discrepancy occurs

* Address correspondence to roman.sordan@como.polimi.it.

Received for review April 18, 2013 and accepted May 28, 2013.

Published online May 28, 2013
10.1021/nn401933v

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because f_T is a measure of internal transistor delays rather than functionality in realistic electronic circuits. Logic gates, as almost all electronic circuits, require FETs with intrinsic voltage gain $A = g_m/g_d > 1$, where g_m is transconductance and g_d is output conductance. Overunity intrinsic gain at room temperature has recently been demonstrated in monolayer graphene FETs incorporated in analog voltage amplifiers[10−12] and digital inverters.[9] Voltage gain larger than unity is needed in logic gates in order to match their input and output signals. Matching allows cascading of logic gates[9] and realization of more complex, realistic circuits, of which the most important class are digital ring oscillators (ROs). ROs are composed of an odd number of inverters (each with two FETs) cascaded in a loop, which provides negative feedback at low frequencies but positive feedback at higher frequencies. The loop makes the RO unstable and therefore induces oscillation at higher frequencies, but only if the inverters satisfy stringent criteria. Each inverter in the loop must be identical, exhibiting overunity voltage gain and in/out signal matching. Moreover, the two FETs in each inverter must exhibit very low on-state resistance to be able to quickly charge/discharge the gate capacitance of the next stage. Since the oscillation frequency $f_o < f_T$ is a direct measure of delays in realistic scenarios, ROs are the standard testbeds for evaluating ultimate performance limits and the highest possible clock rates of digital logic families.[13]

ROs made from strictly low-dimensional materials have previously been demonstrated with carbon nanotubes (CNTs)[14,15] and exfoliated bilayer MoS_2,[16] but not with graphene. In the case of both CNTs and MoS_2, the oscillation frequency was limited by parasitic capacitances and by relatively large on-state resistances of the FETs (>100 kΩ), which limited the oscillation frequencies to 52 MHz (CNTs)[15] and 1.6 MHz (bilayer MoS_2).[16] On the other hand, graphene exhibits large mobility and can be processed by simple fabrication methods on a wafer scale.[17,18] Here we demonstrate high-frequency operation of ROs fabricated from wafer-scale monolayer graphene. The low resistance of graphene FETs (<624 Ω) ensured the highest oscillation frequency (f_o = 1.28 GHz) demonstrated to date in novel low-dimensional materials. The fabricated ROs also represent the first gigahertz multitransistor graphene integrated circuits, which demonstrate the potential for large-scale integration of graphene electronic devices.

RESULTS AND DISCUSSION

A schematic of the investigated ROs is shown in Figure 1a. Graphene monolayers (see Methods) were grown by chemical-vapor deposition (CVD).[19] The ROs were fully integrated on the monolayers (Figure 1b). Complementary operation of the graphene inverters within a RO is obtained between the Dirac points of the

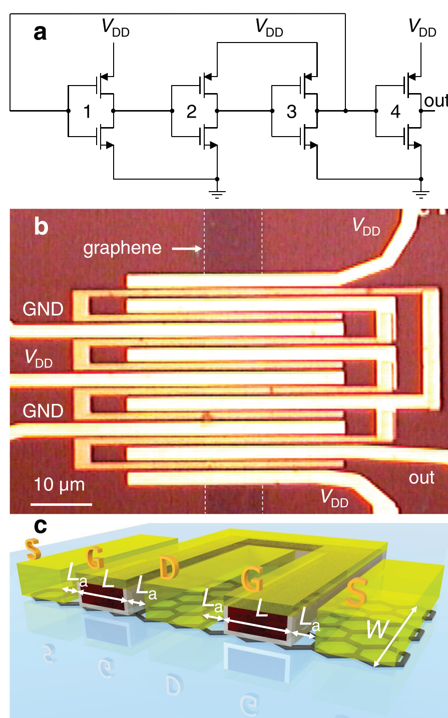

Figure 1. Integrated monolayer graphene ring oscillator (RO). (a) Circuit diagram of a three-stage RO. The RO is composed of three inverters (1−3) cascaded in a loop with the fourth inverter (4) decoupling the RO from the measurement equipment connected to the output (out). (b) Optical microscope image of a small RO (L = 1 μm and W = 10 μm) integrated on the monolayer graphene channel grown by CVD. The drain contacts of inverters 1−3 (Au; bright yellow) overlap with the gate contacts (Al/Ti/Au; orange) in order to form internal connections between the inverters. (c) Schematic of a complementary graphene inverter composed of two FETs. Source (S) and drain (D) contacts (Au; yellow) are separated by a distance L_a from the gate (G) contact (Al; red core), which is covered by an insulating layer (AlO_x; gray shell) and terminated with a conductive layer (Ti/Au; yellow). All inverters in a single RO have the same access lengths (L_a), gate length (L) and width (W). ROs were fabricated with different L and W, but in all cases the access lengths were kept constant (L_a = 0.5 μm).

two FETs,[20] after the supply voltage $V_{DD} > 0$ is applied.[21] In this configuration, the input and output voltages at the highest-gain (*i.e.*, threshold) point of an inverter are mismatched by $V_{IN} - V_{OUT} = V_0$, where V_0 is the voltage at the Dirac point of the unbiased FETs.[9] A positive voltage at the Dirac point (V_0 > 0.2 V, measured in air at room temperature) was found in all fabricated FETs, stemming from p-type doping introduced by ambient impurities adsorbed on graphene.[3,22] Since in/out mismatch at the threshold point rapidly reduces voltage swing in multistage graphene circuits,[9] a positive back-gate voltage, $V_{BG} = (C_{ox}/C_{ox,BG})V_0$, was used to shift the Dirac point back to zero. Here C_{ox} and $C_{ox,BG}$ are the top-gate and back-gate capacitances per unit area, respectively ($C_{ox}/C_{ox,BG}$ = 121.2 and $C_{ox} \approx 1.4$ μF cm^{-2}; see Supporting Information Figure S1). With the appropriate back-gate voltage, the voltage gain of such inverters at the threshold point is $|A_v|$ > 4 (see Figure S2).

Signal matching at the threshold point enables oscillations in a RO if the low-frequency voltage gain satisfies the condition $|A_v| \geq [1 + (\tan(\pi/n))^2]^{1/2}$, where n is the number of inverting stages cascaded in a loop.[23] Three-stage ROs require the highest gain ($|A_v| \geq 2$) compared to ROs with a larger number of stages ($n \geq 5$), but they also oscillate at the highest frequency. As our fabricated inverters satisfy the voltage-gain condition for $n = 3$, three-stage ROs were investigated (as shown in Figure 1) in order to reach high frequencies. The oscillation frequency of a RO depends on the gate delays of the inverters as $1/f_o = 2\sum_{i=1}^{n} \tau_i$ where τ_i is the delay of the ith inverter. Here it is assumed that FETs in an ith inverter are identical, *i.e.*, that both rise and fall time delays are equal to τ_i. In the case of a perfect (*i.e.*, symmetric) RO composed of identical inverters (without the output buffering stage, *i.e.*, inverter 4 in Figure 1a) the expression for frequency simplifies to $f_o = 1/(2n\tau) = f_{o,max}$ where $\tau_i = \tau$ is the gate delay of a single inverter. In a simple transient model (see Supporting Information Section S1) this delay is $\tau = \ln((\sqrt{5} + 1)/2)CG_D^{-1}$ where G_D is the sum of the extrinsic drain conductances of the FETs in the inverter and C is the parasitic capacitive load of the inverter. This load mostly consists of the gate capacitance of the following stage, *i.e.*, $C \approx 3C_G$, where the gate capacitance $C_G \approx LWC_{ox}$ and L and W are the gate length and width, respectively (Section S1). In order to demonstrate scaling of such circuits, we fabricated three types of graphene ROs: large (L = 3 μm and W = 20 μm), medium (L = 2 μm and W = 10 μm), and small (L = 1 μm and W = 10 μm). Typical values for G_D and C_G of these three types of ROs are given in the Supporting Information Table S1. With n = 3 and these parameter values, the simulations presented in Section S1 would lead us to expect $f_{o,max}$ = 457 MHz for large ROs, $f_{o,max}$ = 811 MHz for medium ROs, and $f_{o,max}$ = 2.08 GHz for small ROs (Table S1).

Figure 2 shows voltage signals measured at the output of the three types of fabricated ROs with the buffering stage. In all three cases the oscillation frequencies are smaller than the respective $f_{o,max}$ because the buffering inverter introduces an additional capacitive load on the inverter to which it is connected. This additional load reduces the oscillation frequency to $f_o \approx f_{o,max} \ln(2 + \sqrt{5})/\ln(3 + 2\sqrt{2}) < f_{o,max}$ (Section S1). This yields f_o = 359 MHz for large ROs, f_o = 648 MHz for medium ROs, and f_o = 1.76 GHz for small ROs. The first two values are very close to the measured frequencies of 350 MHz (large RO) and 618 MHz (medium RO) shown in Figure 2. Only in the case of small ROs does the model overestimate the frequency because it does not account for all parasitic capacitances that dominate at smaller device sizes. The measured oscillation frequency scales approximately with $1/L$ mostly because G_D^{-1} does not scale with L/W due to contact resistances (which scale only with $1/W$) and the

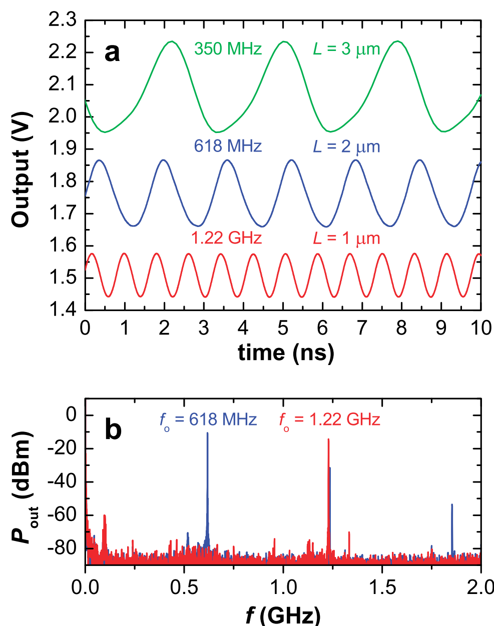

Figure 2. Output signals of buffered graphene ROs at V_{DD} = 3.5 V. (a) Large RO (green; L = 3 μm and W = 20 μm) oscillates at 350 MHz at V_{BG} = 34 V (see text). The voltage swing is V_{p-p} = 0.284 V. Medium RO (blue; L = 2 μm and W = 10 μm) oscillates at 618 MHz at V_{BG} = 5 V. The voltage swing is V_{p-p} = 0.208 V. Small RO (red; L = 1 μm and W = 10 μm) oscillates at 1.22 GHz at V_{BG} = 50 V. The voltage swing is V_{p-p} = 0.136 V. The voltage swing is strongly suppressed by the low-pass filtering of the buffer (see Sections S2, S3). The green and red curves are vertically offset for clarity, from the midpoint voltage $V_{DD}/2$ = 1.75 V. (b) Respective power spectra of the medium and small ROs. The second harmonic of the medium RO is at the position of the first harmonic of the small RO.

parasitic resistances and capacitances of the interconnects, which do not scale (statistics and scaling of the 26 working ROs are shown in Figure S9). In general, the fabricated buffered ROs exhibited oscillation frequencies in the range 284 MHz < f_o < 350 MHz (large ROs), 504 MHz < f_o < 750 MHz (medium ROs; Figure S14), and 1 GHz < f_o < 1.28 GHz (small ROs; Figure S14). The variability of f_o stems from variations in overlap resistances between the input and outputs of the inverters (which influence f_o through G_D). The largest voltage swing in fabricated ROs was 0.57 V (Section S2). All three ROs shown in Figure 2 required relatively low back-gate voltages (as low as V_{BG} = 5 V) and were operated in ambient air.

The oscillation frequency of conventional ROs, as well as those made from nanomaterials such as CNTs and MoS_2, strongly depends on the supply voltage V_{DD}. This represents a serious problem in complex digital circuits in which a large number of transistors and increased power consumption place increased demand on the voltage supply, causing it to fluctuate.[24] Such fluctuations not only have a negative impact on the operation of logic gates but also deteriorate their noise performance.[24] We found that, in contrast to other types of ROs, graphene ROs are much less

sensitive to fluctuations in the supply voltage. Figure 3 shows the power spectrum of the output signal (oscillating at $f_o \approx 700$ MHz) in a buffered RO at different supply voltages. At larger supply voltages both voltage swing and oscillation frequency are larger. Voltage swing increases with supply V_{DD} because a larger unity-gain voltage swing is obtained at larger supply voltages.[9] The increase in oscillation frequency is a consequence of an increase in the total drain conductance of graphene FETs at larger V_{DD} (as $f_o \propto G_D$). Although such a dependence of f_o on V_{DD} exists in all types of ROs, it is much weaker in the case of graphene ROs due to much weaker dependence of G_D on V_{DD} in graphene FETs (Section S4). For the RO shown in Figure 3, the change of oscillation frequency with supply voltage is ~5.6%f_o/V on average. This is about 7, 21, and 51 times smaller than that of ROs based on Si CMOS (Figure S16), MoS_2,[16] and CNTs,[15] respectively. Such a weak dependence in graphene ROs could be a disadvantage in applications in which dynamic frequency and voltage scaling are used to throttle down digital circuits during periods of reduced workload. However, insensitivity of graphene ROs to power supply noise represents an important advantage in applications in which frequency stability is of the utmost importance, *e.g.*, for clock generation in high-speed digital systems.

The fabricated ROs can also be used in analog applications such as frequency mixing.[25] Graphene analog mixers[26,27] have recently been suggested as one of the possible applications of graphene in high-frequency analog electronics, since frequency mixing does not require devices that exhibit overunity voltage gain. However, without voltage gain the signals cannot be amplified (which is necessary for signal transmission), nor is it possible to generate oscillating signals. For this last reason, the graphene mixers that have so far been demonstrated[26−29] have required an external local oscillator (LO) for frequency conversion. The ROs demonstrated here can overcome these limitations and perform both modulation and generation of oscillating signals to form stand-alone graphene mixers, *i.e.*, mixers with a built-in LO. To this end, the RO shown in Figure 1a was modified by superimposing a radio frequency (RF) signal $v_{rf}(t) = V_{rf} \sin(2\pi f_{RF} t)$ over the dc supply V_{DD} of the decoupling inverter 4 (without affecting the supplies of the other three inverters, Figure S17); hence $v_{DD4}(t) = V_{DD} + v_{rf}(t)$. As the other three inverters forming a ring are not affected by the addition of the RF signal, the alternating current (ac) component of the oscillating voltage at the input of the fourth inverter is also unaltered, which is to a first approximation $v_{in4}(t) \approx V_{in4} \sin(2\pi f_{LO} t)$, where $f_{LO} = f_o$. The RF signal modulates the supply of the fourth inverter and thereby changes its voltage gain. Assuming a linear relationship between A_{v4} and $v_{DD4}(t)$,[12] the voltage gain is $A_{v4}(v_{DD4}) = A_{v4}(V_{DD}) - kv_{rf}$, where k is the proportionality

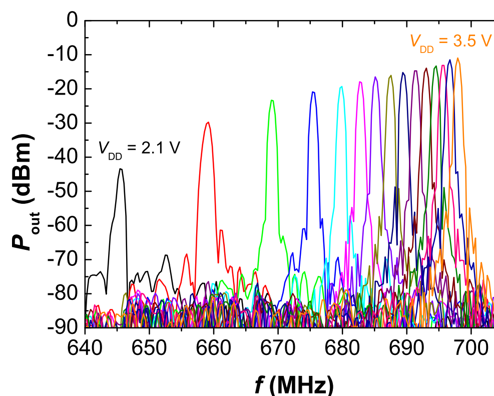

Figure 3. Power spectrum of the output signal measured in a medium-size buffered RO (L = 2 μm and W = 10 μm) at different supply voltages as labeled, and V_{BG} = 89 V. From left to right: V_{DD} = 2.1 to 3.5 V in steps of 0.1 V. At larger V_{DD} the drain conductance increases more slowly, and therefore the oscillation frequency increases more slowly with the increase of V_{DD}. This results in reduced spacing between the maxima in the power spectrum at larger V_{DD}.

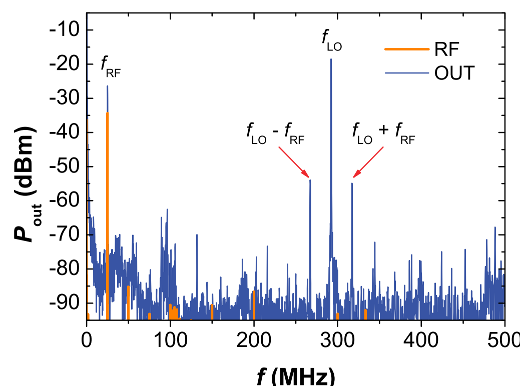

Figure 4. Power spectrum of the input (RF) and output (OUT) signals of the stand-alone graphene mixer at V_{DD} = 2.5 V and V_{BG} = 166 V. The signal frequencies are f_{LO} = 292 MHz and f_{RF} = 25 MHz. Apart from the signals discussed in the main text, the output signal also contains a frequency component at f_{RF}, which comes from the amplification of the RF signal by the inverter 4. The output signal in the time domain is shown in Figure S18.

factor ($k \approx 2$ V^{-1}). The ac component of the output signal is then $v_{out}(t) = A_{v4} v_{in4} = A_{v4}(V_{DD}) v_{in4} - k v_{rf} v_{in4}$.

Figure 4 shows the power spectrum of the output signal in which both terms from the previous expression can be seen. The first term is the signal of the LO at a frequency f_{LO}, whereas the second term is the product of the LO and RF signals $\propto \sin(2\pi f_{RF} t) \sin(2\pi f_{LO} t)$, which gives rise to intermediate frequencies $f_{LO} \pm f_{RF}$. At larger amplitudes of the RF signal nonlinear intermodulation of the RF and LO signals will generate intermediate frequencies $l f_{LO} \pm m f_{RF}$, where l and m are integers (Figure S19). In this case, the circuit will act as a harmonic mixer. The conversion loss obtained from Figure 4 is 19.6 dB at an LO power of −18.5 dBm and RF power of −34.3 dBm, which is better than in early graphene mixers,[26,27] but worse than in recent graphene mixers.[28,29] Also, the isolation between the

mixer ports is insufficient (*e.g.*, the RF port is not isolated from the LO signal). However, both conversion loss and port isolation could be improved with the current technology, as fabricated inverters exhibit voltage gain. By feeding the RF signal through an additional inverter (*i.e.*, an amplifier) the conversion loss could be reduced and the influence of the LO signal at the RF port could be suppressed. In general, conversion loss is not a critical parameter, as low-gain mixers usually exhibit better noise figures and linearity than high-gain mixers. Required signal levels in the former case are often obtained by filtering the output before passing it to an additional low-noise amplifier stage.

There are several figures of merit that should be considered before graphene can be used in digital applications. The absence of a band gap in graphene results in a nonzero off-state drain current, which leads to considerable static power dissipation. The typical static drain current in our small graphene inverters is $I_D/W \approx 270\ \mu A/\mu m$ at $V_{DD} = 2.5$ V, in contrast to much smaller leakage drain current $I_D/W \approx 100$ nA/μm at $V_{DD} = 0.75$ V in 22 nm node high-performance silicon logic transistors.[30] This prohibits the use of graphene in highly integrated low-power digital applications (such as Si CMOS), even though leakage power also exceeds dynamic (switching) power in most state-of-the-art Si logic circuits.[31,32] Lack of a band gap also reduces the voltage swing in graphene inverters, which together with their nonsaturated transfer curves reduces the noise margin (Figure S20). Finally, in order to reach a voltage gain of >1, the gate oxide thickness in graphene FETs must be more aggressively scaled than the gate length and supply voltage, breaking the conventional scaling laws. The present oxide thickness (~4 nm) is only slightly larger than that of contemporary Si FETs, and in both cases further scaling benefits can be obtained only at the expense of other advances (*e.g.*, use of high-*k* oxides, fins, and strain engineering). The only advantage of graphene ROs with respect to Si CMOS ROs is a smaller sensitivity to supply fluctuations; however, this comes as a consequence of the reduced voltage swing. The graphene ROs also exhibit larger phase noise than Si ROs (Figure S21).

Graphene can find applications in EHF digital circuits in which large charge carrier mobility leads to high operating speed, which could be traded off against power dissipation, reduced voltage swing, and circuit complexity.[7,33−35] However, before graphene can be considered as a replacement for InP heterojunction bipolar transistors in EHF applications, further technological advances are needed. The inverter delay in the fabricated ROs with $L = 1\ \mu m$ is $\tau \approx 100$ ps, which is similar to that of Si CMOS inverters at the same gate length.[36] This is a consequence of similar *extrinsic* charge carrier mobilities ($\mu \approx 500\ cm^2\ V^{-1}\ s^{-1}$) in these two cases. Such low extrinsic mobility of graphene (compared to its intrinsic mobility, which is much larger than that of Si and InP) is a consequence of a large contact resistance (here ~2 k$\Omega\cdot\mu$m) and scattering from charged impurities in the top and back oxide. Both contact resistance and impurity scattering must be reduced if graphene is to replace InP in future EHF circuits. Higher mobility will also allow lower supply voltages, thus reestablishing conventional scaling laws. However, graphene can immediately find applications in analog electronics. Oscillators are one of the main building blocks of analog electronics,[37] *e.g.*, RF (microwave) electronics is built on voltage amplifiers, oscillators, and mixers.[25,38] Amplifiers[11,12] and mixers[26,27] have already been demonstrated, and the oscillators demonstrated in this work represent the final missing component for the realization of all-graphene microwave circuits. Finally, graphene electronic circuits can be used on transparent and flexible substrates that are inaccessible to conventional semiconductors.

CONCLUSIONS

In summary, we have demonstrated integrated graphene ROs operating at room temperature, under ambient conditions. The ROs were fabricated from wafer-scale CVD monolayer graphene and were composed of inverters exhibiting signal matching and large voltage gain, $|A_v| > 4$. The fabricated ROs oscillate at the highest frequency (1.28 GHz) reported to date in a strictly low-dimensional transistor material, with the voltage swing (as a fraction of supply voltage) exceeding that of conventional InP ECL gates, the fastest logic family. Graphene ROs are more robust to variations in supply voltage compared to conventional ROs and could be used in applications where ultrafast operation is favored over static power dissipation. We also realized the first graphene stand-alone mixers as a simple demonstration of versatility of the fabricated ROs. Oscillation frequency could be increased through further advances, *e.g.*, by reducing the FET channel length, contact resistance, and parasitic capacitances. Even static power dissipation could be reduced by increasing the voltage swing through the use of AB-stacked bilayer graphene[39−42] once such material becomes available at a wafer scale. The fabricated ROs are an important step toward the application of graphene in electronics.

METHODS

Graphene monolayers (Figure S22) were grown by CVD on Cu with a CH_4 precursor and transferred to SiO_2 (300 nm)/Si substrates. Graphene transistors were patterned by e-beam lithography and reactive-ion etching, whereas the contacts were deposited in an e-beam evaporator. Source and drain

contacts consisted of Au (75 nm), and the gate was made of Al/Ti/Au (45/2/13 nm). The back of the Si substrates was metalized and used as a global back-gate, if needed. Top-gates were fabricated by direct evaporation of Al on graphene, which upon exposure to air naturally forms a very thin (~4 nm) AlO_x gate insulator at the interface with graphene.[21] However, because oxidation would also form an insulating layer on the top surface of the gates, they were terminated with a thin layer of Ti/Au during the same evaporation step (Figure 1c). This approach allowed the formation of ohmic contacts between the gates of one stage and the source/drain terminals of another (Figure 1b). Such internal connections between the output of each inverter and the input of the following inverter significantly reduce parasitic capacitances in the circuit and consequently increase the oscillation frequency. However, the presence of a conductive layer on the top surface of the gates prevents self-alignment of the contacts[9,12] and therefore introduces unwanted access resistances, which reduce the voltage gain. In order to preserve the voltage gain, we reduced the source/drain access resistance by contacting the graphene with purely Au contacts, without the use of a Ti or Cr adhesion layer (Figure S23). Thus, despite the lack of perfectly self-aligned contacts, we were nevertheless able to recover a voltage gain of $|A_v| > 4$ (Figure S2), similar to previous work on self-aligned FETs in which a Ti adhesion layer was used below the Au contacts.[9] Typical dc transfer characteristics are shown in Figure S20.

The circuit layout shown in Figure 1b uses two ground and three V_{DD} supply lines instead of single ground and V_{DD} leads used in typical integrated circuits. This circuit layout was chosen for two reasons: First, it eliminated two extra fabrication steps to realize isolation in the overlap regions between the dc lines. Second, the measurements shown in Figure S17 (mixer) and Figure S2c would not be possible with a single V_{DD} line. A complete circuit layout is shown in Figure S24.

A positive voltage at the Dirac point was found in all fabricated FETs, and therefore a positive back-gate voltage was used to shift the Dirac point back to zero, as described in the main text. Although this allows oscillations in samples with arbitrary large initial Dirac voltages, we found that most of the samples that required large back-gate voltages to oscillate (V_{BG} > 100 V) did not exhibit long-term stability in ambient air. This was due to a back-gate hysteresis that was found to shift the Dirac point of the FETs to larger back-gate voltages even after the Dirac point was shifted to zero (Figures S25−S26). Such samples cannot be used in realistic applications, emphasizing the need for low sample doping.[9] The samples shown in the main text exhibited long-term stability (*e.g.*, the medium RO from Figure 2 also oscillated at zero back-gate voltage). That is, the back-gate voltage was needed only for samples that had high levels of unintentional doping, and it was therefore entirely unnecessary in very clean samples.

All measurements were performed at room temperature. ROs that required low (or zero) back-gate voltages were operated in air. ROs that required large back-gate voltages could not achieve long-term stability without reducing their exposure to air. Although this could be achieved under vacuum, this was not attempted as vacuum is not a typical operating environment of electronic devices and was also found to reduce the voltage gain of the inverters.[9] Instead, such ROs were operated in air under N_2 flow. The voltage signals were measured by Agilent Infiniium DSO9064A (bandwidth 600 MHz) and DSO9254A (2.5 GHz) digital storage oscilloscopes, while the RF signal was generated by a Tektronix AFG 3022B function generator. In order to minimize the parasitic capacitive load of the ROs, the outputs were connected to the oscilloscope *via* Agilent N2795A (bandwidth 1 GHz, capacitance 1 pF), N2796A (2 GHz, 1 pF), and 1158A (4 GHz, 0.8 pF) active probes.

Conflict of Interest: The authors declare no competing financial interest.

Acknowledgment. We thank M. Ahangarianabhari for useful discussion and M. Leone and A. Lena for technical support. This research was supported in part by Fondazione Cariplo, grant no. 2011-0373 and Directa Plus srl, and by the United States Office of Naval Research (ONR) and Air Force Office of Scientific Research (AFOSR).

Supporting Information Available: Measurements and discussions on top-gate capacitance, dc characteristics of individual FETs and inverters, extensive modeling and simulations of the fabricated ROs, scaling of the oscillation frequency, detuning of the ROs, the highest frequencies and voltage swings of the fabricated ROs, higher harmonics, output bandwidth, influence of the supply voltage on the oscillation frequency, circuit diagram and output signals in the time domain of the standalone graphene mixers, nonlinear intermodulations in the mixers, noise margin, phase noise, Raman spectrum of monolayer graphene, contact resistance, complete circuit layout, back-gating used to shift the Dirac point, and drift of the transfer curves at large back-gate voltages. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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